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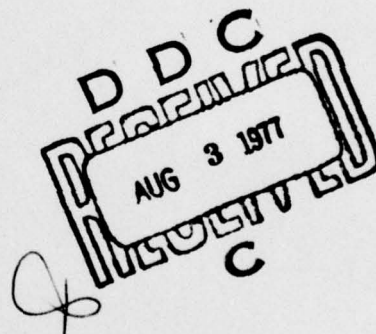
Microwave Frequency Division Over Octave Bands

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C. W. WALLACE

*Offboard Countermeasures Group
Tactical Electronic Warfare Division*

June 1977



NAVAL RESEARCH LABORATORY
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) In many areas of electronic system design and engineering, there exists a need for improved methods of processing microwave frequencies. A key component in future designs could be a broad-band frequency divider. This report discusses a divide-by-two circuit utilizing regenerative modulation having an input frequency range of 500 MHz to 1 GHz and a similar circuit having an input frequency range of 250 MHz to 500 MHz that were developed. When the two circuits are cascaded the net result is a device that will accept any signal between 500 MHz and 1000 MHz (pulsed or cw)		

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20. Abstract (Continued)

and provide an output equal to the input frequency divided by four. Outstanding features of the circuits are the ability to down-convert a band of frequencies while maintaining the same bandwidth percentage, the ability to maintain a fixed phase relationship with a given input frequency, and operation over wide frequency ranges.

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The author would like to acknowledge that the regenerative technique for achieving division at microwave frequencies and its potential usefulness in electronic warfare was pointed out by E.E. Kempe of the Advanced Techniques Branch, Tactical Electronic Warfare Division, Naval Research Laboratory.

MICROWAVE FREQUENCY DIVISION OVER OCTAVE BANDS

1.0 INTRODUCTION

With the relatively recent development of broad-band components such as amplifiers, mixers, and couplers frequency division can now be accomplished over a wide range of microwave frequencies. A previous investigation conducted by Miller¹ was done at very low frequencies. In this article credit for the basic idea is given to Horton². G. Immovilli and G. Montovani³ evaluated the effects of phase shift in the feedback loop of a Miller frequency divider.

This report will be limited to a discussion of circuits designed to operate over an input frequency range of 500 MHz to 1 GHz and 250 MHz to 500 MHz for which the design considerations, test results, and appropriate conclusions are presented. Each divide-by-two circuit is evaluated individually, and then the two circuits are cascaded to form a divide-by-four device and results reported.

2.0 PURPOSE OF INVESTIGATION

This investigation was conducted primarily to determine if a device could be developed that would exactly divide a wide range of frequencies by two and if so to evaluate both the desirable and undesirable features.

There are many practical uses for a device that has the ability to convert a wide range of frequencies to a band of

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equal percentage at lower frequencies, at which many operations are more easily performed. If it were then desirable to convert back to the original input frequency, this could easily be accomplished with frequency doublers and amplifiers which are readily available commercially.

This investigation has been ongoing for approximately two years, however it was conducted at a low level due to higher priority responsibilities assigned to the author.

3.0 THEORY OF OPERATION

The theory of operation of the divide-by-two circuits discussed in this article can probably be best explained with reference to the circuit diagram shown in Fig. 1, which consists of a mixer, amplifier, filter and coupler.

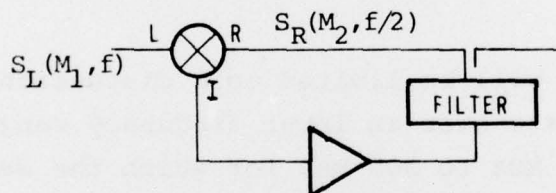


Fig. 1 — Basic block diagram of frequency divider

In the above diagram, a mixer is shown having the I.F. port fed to an amplifier, the output of which is fed to a filter which in turn is fed to the R port through a coupler. If a signal $S_L(M_1, f)$ of magnitude M and frequency f is applied to the L port of the mixer and value of M_1 is sufficient to approximate the required LO drive level for the given mixer, then any signal present at the R port will cause the sum and difference frequencies of these two signals to appear at I port. If the signal present at the R port were to have a frequency of $f/2$ and magnitude of M_2 , then the sidebands present at the

I port would consist of $S_I \left[(\gamma M_2, f/2); (\gamma M_2, 3 f/2) \right]$ where γ is the conversion loss factor of the mixer. The sideband at $3 f/2$ is attenuated by the filter and will be given no further consideration. If the gain of the amplifier exceeds the combined losses of the mixer, filter, and coupler, then the signal at $f/2$ will be reapplied to the R port delayed in time by the propagation delay of the feedback loop, but at a level exceeding the original magnitude M_2 . Due to this regenerative action the signal at $f/2$ will eventually reach a magnitude sufficient to cause gain compression in either the amplifier or the mixer.

For purposes of this report, it is assumed that starting oscillation takes place due to the presence of $S_R (M_2, f/2)$ at the input in the form of thermal noise. A more detailed discussion of the principle of regenerative modulation can be found in reference (1).

4.0 DESIGN CONSIDERATIONS AND CIRCUIT DESCRIPTION

The frequency ranges over which the two circuits operate were chosen for these reasons:

- The author has had considerable circuit design experience from D.C. to 1 GHz.
- 500 MHz to 1 GHz is a frequency range in which the divider will have practical value.
- The 250 MHz to 500 MHz band was chosen so as to be compatible with the output of the 500 MHz to 1 GHz device.
- Low cost of components.

The diagram of Fig. 2 serves to represent both the 250 MHz - 500 MHz divider and the 500 MHz to 1 GHz divider. Each circuit was constructed on a metal plate and mounted in a metal box 2" x 4".

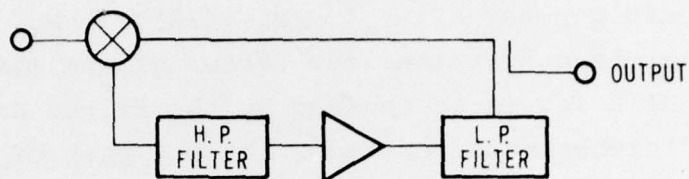


Fig. 2 — Block diagram of circuit

The same model mixer, amplifier and coupler were used for both frequency ranges as both are broad-band general purpose components.

Pertinent specifications for these components are:

- Mixer

Conversion loss - 7 db maximum

Isolation - LO and RF to IF = 20 db minimum

Frequency range at R and L Port - 5 MHz to 1 GHz

Frequency range at I Port - D.C. to 1 GHz

- Amplifier

Frequency range - 5 MHz to 500 MHz

Gain - 10 db minimum

Gain Flatness $\pm .5$ db

- Coupler

Nominal coupling - 11 db typical

Main line loss - 1.6 db maximum

- Filters*

In the 250 MHz to 500 MHz circuit the high-pass filter is a two-pole type designed for linear phase characteristics above 125 MHz and the low-

*Several sections of both high- and low-pass filters for both circuits were included in the original design, but it became apparent during the early part of the investigation that phase characteristics in the loop were more important than good frequency selectivity.

pass filter is a three-pole type designed for linear phase below 250 MHz.

For the 500 MHz to 1 GHz circuit the high-pass filter is of the RC type. No filtering other than the natural roll-off of the amplifier was used for high frequency attenuation.

5.0 TEST RESULTS

All measurements and photographs referred to under this section have reference to Fig. 3.

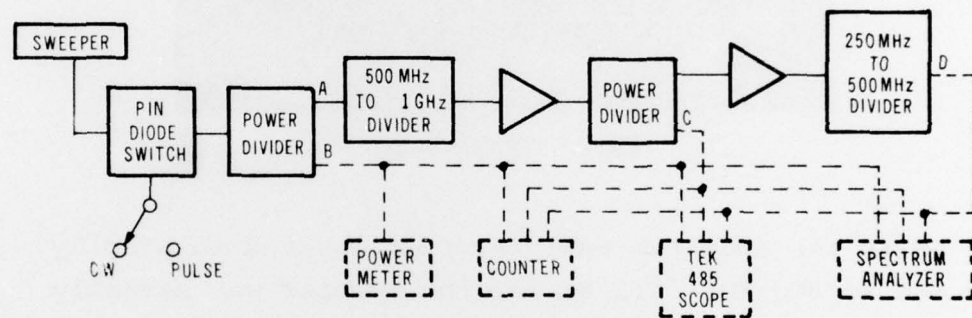


Fig. 3 — Block diagram of test configuration

With the spectrum analyzer calibrated to display 75 MHz per division (250 MHz to 1 GHz full scale) Fig. 4 shows the output of the 500 MHz to 1 GHz divider at point C of Fig. 3 with a +6 dbm cw signal (650 MHz) applied to point A. Toward the left side of the screen is the desired output $f/2$ (325 MHz). Slightly to the right of the center of the screen is the input signal at 650 MHz and toward the right side of the screen is $3 f/2$ (975 MHz).

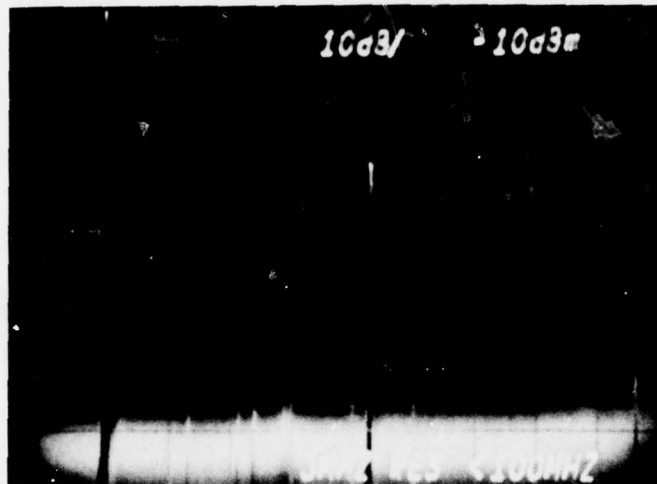


Fig. 4 — Typical output

With the spectrum analyzer recalibrated to display 250 MHz to 500 MHz full scale, the sweeper was manually tuned through the 500 MHz to 1 GHz frequency range to determine at what input frequency spurious responses occurred in the output pass band and the level of these spurious responses relative to the desired output ($f/2$). This procedure was followed with the input level incremented in 1 db steps between +2 dbm and +7 dbm. The worst-case spurious response was found to be with the input signal at a frequency of 950 MHz and a power level of +7 dbm. The worst-case spurious response over the entire operating range of the device is 45 db below the desired output as illustrated in Fig. 5.

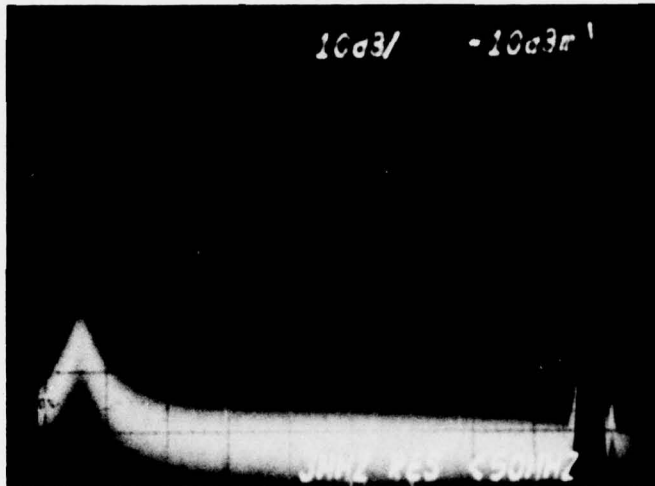


Fig. 5 — Spurious response of the 500 MHz
to 1 GHz divide-by-two circuit

As will be the case in all frequency dividers designed to operate over an octave band, the input frequency will appear at the output when the input is at the frequency where the bands overlap. Figure 6 illustrates the rejection to an input frequency of 500 MHz which is the worst-case for the 500 MHz to 1 GHz divider being discussed.

With the spectrum analyzer still calibrated to display 250 MHz to 500 MHz, a 500 MHz cw signal at +6 dbm is applied to point A. From Fig. 6 it can be seen that the magnitude of the input signal appearing in the output is greater than 30 db below the desired output at 250 MHz (left side of display).

This is a tribute to the isolation of the mixer.

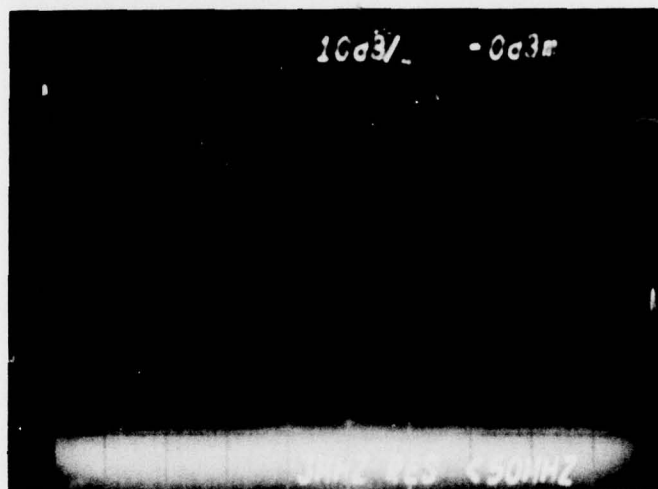


Fig. 6 — Isolation of 500 MHz to 1 GHz
divide-by-two circuit

The 250 MHz - 500 MHz divider was found to be stable over its entire frequency range at all input levels between 0 dbm and +7 dbm. Worst-case spurious responses for this band were also 45 db below the desired output at any input level between 0 dbm and +7 dbm and occurred at an input frequency of 288 MHz.

Again referring to Fig. 3 the spectrum analyzer was calibrated to display 125 MHz to 250 MHz full scale and connected to point D. With the sweeper manually tuned from 500 MHz to 1 GHz, a corresponding divide-by-four output was observed at all input frequencies at any power level between +2 dbm and +7 dbm.

Figure 7 shows the divide-by-four output (125 MHz) observed at point D with an input signal at 500 MHz. The

250 MHz signal at the right of the display is indicative of mixer isolation at 250 MHz.

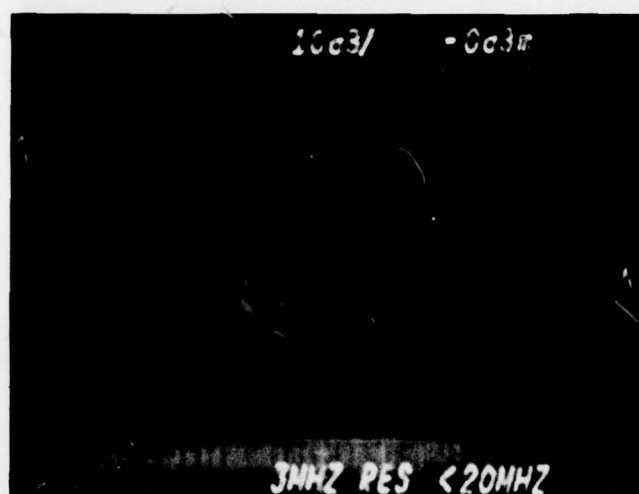


Fig. 7 — Divide-by-four output containing $f/2$

Figure 8 displays the worst-case spurious response observed at the divide-by-four output. This occurred with an input signal of 576 MHz, and again was found to be 45 db below the desired output.

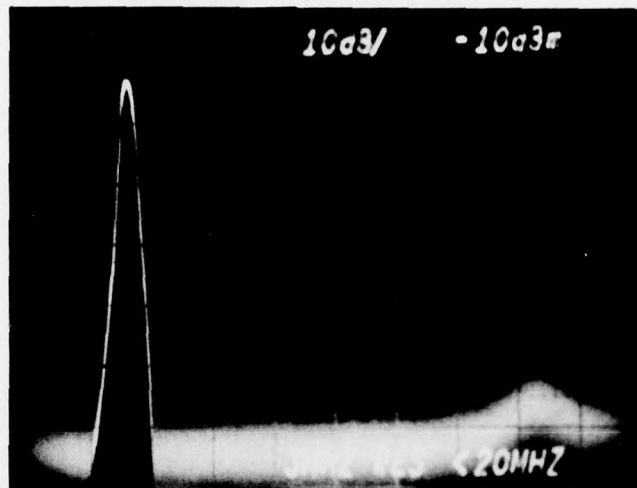


Fig. 8 — Spurious response at
divide-by-four output

Figure 9 illustrates the behavior of the 500 MHz to 1 GHz divider with a pulsed type signal applied. Again referring to Fig. 3 a signal at 630 MHz gated on for a period of 100 ns at a rate of 50 KHz is applied to point A. The lower trace of the oscilloscope shows the input signal as observed at point B. The upper trace shows the output of the divide-by-two circuit as observed at point C. The horizontal time base was set at 20 ns per division.

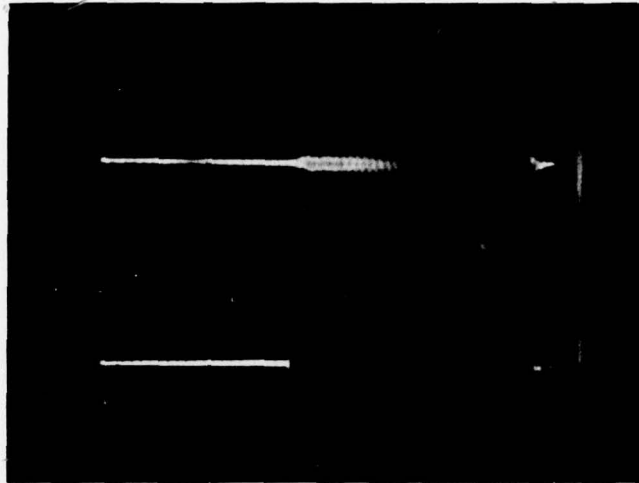


Fig. 9 — 500 MHz to 1 GHz divide-by-two
circuit response to pulsed signal

The important fact illustrated by Fig. 6 is that for a given closed-loop gain, ≈ 60 ns is required for the circuit to reach a stable amplitude at $f/2$ when the input frequency is 630 MHz.

The pulse width was increased to 200 ns and the sweeper was tuned manually from 500 MHz to 1 GHz. It was observed that the time required for the divide-by-two output to reach equilibrium varied between 40 ns and 125 ns.

With the sweeper remaining at 630 MHz, but the pulse width increased to 200 ns at a 50 KHz rate, and horizontal time base changed to 50 ns per division the photograph of Fig. 10 shows the divide-by-two output on the upper trace and the divide-by-four output on the lower trace. This photograph illustrates that the divide-by-four output does not reach maximum amplitude until approximately 90 ns after the divide-by-two output has reached maximum amplitude.

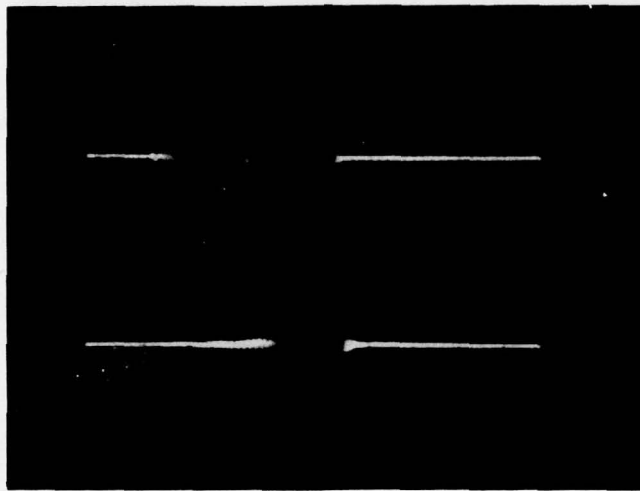


Fig. 10 — $f/4$ with respect to $f/2$

To determine the variations in stabilization time over the entire input frequency range, the pulse width was increased to 300 ns and the sweeper was tuned manually from 500 MHz to 1 GHz. It was observed that the time required for the divide-by-four output to reach maximum amplitude varied between 70 ns and 250 ns.

The photograph of Fig. 11 is included to show that the output of the 500 MHz to 1 GHz divide-by-two circuit is primarily sinusoidal.

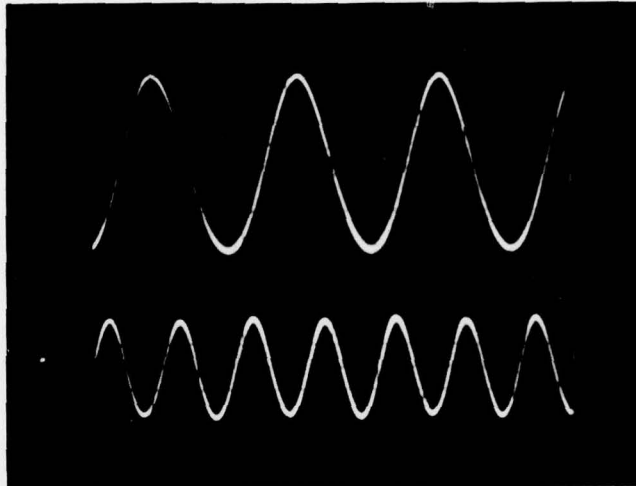


Fig. 11 — 500 MHz to 1 GHz divide-by-two
output vs input

With the horizontal time base set at 1 ns per division the upper trace shows the output as observed at point C while the lower trace shows the input signal (630 MHz) applied to point A.

6.0 CONCLUSIONS

As was mentioned previously, during the course of the experiment several different filter designs were tried in the feedback loop of both bands. It was determined that the higher the complexity of the filters (designed for best-shape factor) the more critical loop gain and input level became. Although the circuits would divide by two over their entire operating range spurious responses could not be reduced to an acceptable level. The results reported were

achieved by minimizing both the physical and electrical length of the feedback loop.

The spurious signals were not positively identified but it was determined that they were not strictly a multiple or a fraction of the input frequency alone or any product of this combination.

Based on the results reported and other observations, it is believed that a number of divide-by-two circuits can be cascaded with the level of the spurious responses determined by the final divider circuit.

The wide variations in delay time or time required for divider output to build up to a stable amplitude value are due primarily to closed-loop gain variations as a function of frequency. It is believed that if the circuits discussed in this article were to be redesigned in the form of an integrated circuit to reduce physical size and therefore propagation delay, the time required for the divider output to build up to a stable amplitude value would be reduced considerably. In addition, if more emphasis were placed on optimizing closed-loop gain variations over the entire frequency, delay time variations could be minimized.

7.0 RECOMMENDATIONS

In view of the encouraging performance of the 500 MHz to 1 GHz divide-by-two and divide-by-four circuits discussed, it is felt that development of other dividers that would provide continuous coverage between 1 GHz and 16 GHz (in octave bands) should be pursued.

The ability to divide 8 GHz - 16 GHz to equal percentage lower frequency bands would be of high value to several programs that are presently ongoing in the Offboard Counter-measures Group.

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2. U.S. Patent No. 1690299
3. G. Immovilli and G. Montovani "Analysis of the Miller Frequency Divider by Two in View of Applications to Wide Band F.M. Signals", Alto FREQUENZA Vol. 42, November 1973